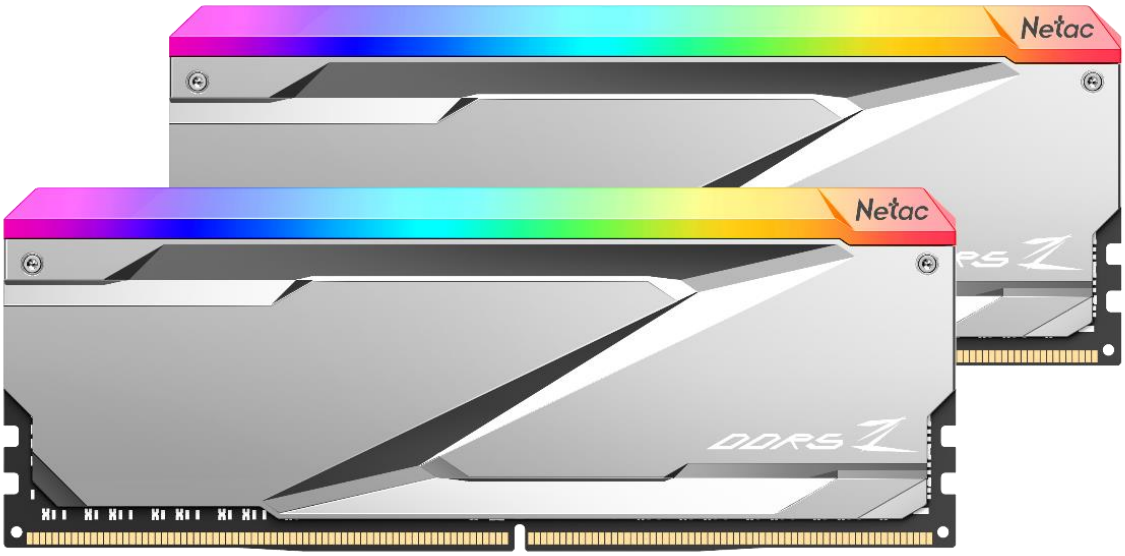
Z RGB DDR5 UDIMM
Memory Module Specifications



Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	Sep. 2022	
1.1	Added Model	Feb. 2023	

Ordering Information Table

Model	Type	Capacity	Speed	Latency	Voltage
NTZED5P80DP-32S	DDR5 UDIMM	32GB (16GB x 2)	8000MHz	38-48-48-128	1.5V
NTZED5P76DP-32S	DDR5 UDIMM	32GB (16GB x 2)	7600MHz	36-46-46-122	1.4V
NTZED5P72DP-32S	DDR5 UDIMM	32GB (16GB x 2)	7200MHz	34-45-45-115	1.4V
NTZED5P66DP-32S	DDR5 UDIMM	32GB (16GB x 2)	6600MHz	34-40-40-105	1.4V
NTZED5P62DP-32S	DDR5 UDIMM	32GB (16GB x 2)	6200MHz	32-38-38-96	1.35V
NTZED5P60DP-32S	DDR5 UDIMM	32GB (16GB x 2)	6000MHz	36-36-36-96	1.35V

Description

Netac Unbuffered DDR5 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR5 SDRAM devices. Each 288- pin DIMM uses gold contact fingers. The SDRAM Unbuffered DIMM is intended for use as main memory when installed in systems such as PCs.

Features

- Adjustable RGB lighting effects
- 32 Bank with x4/x8 / 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Same Bank Refresh
- Input Clock Frequency Change
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Connectivity Test (CT) / ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- On-Die ECC
- CRC (Cyclic Redundancy Check)
- Package Output Driver Test Mode
- Training Modes:
  - VrefDQ / VrefCA / VrefCS Training
  - Read Training Mode
  - CA Training Mode
  - CS Training Mode
  - Per Pin VREFDQ Training
  - Write Leveling Training Mode
  - Duty Cycle Adjuster (DCA) for Read – Global
  - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)
- PCB: Height 1.23” (31.25mm)
- RoHS Compliant and Halogen-Free

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Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	73	CK0_A_c	145	VIN_BULK	217	CK1_A_c
2	RFU	74	VSS	146	VIN_BULK	218	VSS
3	RFU	75	RFU	147	PWR_GOOD	219	RFU
4	HSCL	76	RFU	148	HSA	220	RFU
5	HSDA	77	VSS	149	RFU	221	VSS
6	VSS	78	CK0_B_t	150	VSS	222	CK1_B_t
7	RFU	79	CK0_B_c	151	PWR_EN	223	CK1_B_c
8	VSS	80	VSS	152	RFU	224	VSS
9	DQ0_A	81	RFU	153	VSS	225	RFU
10	VSS	82	CA12_B	154	DQ2_A	226	RFU
11	DQ1_A	83	VSS	155	VSS	227	VSS
12	VSS	84	CA10_B	156	DQ3_A	228	CA11_B
13	DQS0_A_c	85	CA8_B	157	VSS	229	CA9_B
14	DQS0_A_t	86	VSS	158	DM0_A_n	230	VSS
15	VSS	87	CA6_B	159	VSS	231	CA7_B
16	DQ4_A	88	CA4_B	160	DQ6_A	232	CA5_B
17	VSS	89	VSS	161	VSS	233	VSS
18	DQ5_A	90	CA2_B	162	DQ7_A	234	CA3_B
19	VSS	91	CA0_B	163	VSS	235	CA1_B
20	DQ8_A	92	VSS	164	DQ10_A	236	VSS
21	VSS	93	CS0_B_n	165	VSS	237	CS1_B_n
22	DQ9_A	94	VSS	166	DQ11_A	238	VSS
23	VSS	95	RESET_n	167	VSS	239	DQS4_B_c
24	DM1_A_n	96	VSS	168	DQS1_A_c	240	DQS4_B_t
25	VSS	97	CB0_B	169	DQS1_A_t	241	VSS
26	DQ12_A	98	VSS	170	VSS	242	CB2_B
27	VSS	99	CB1_B	171	DQ14_A	243	VSS
28	DQ13_A	100	VSS	172	VSS	244	CB3_B
29	VSS	101	DQ0_B	173	DQ15_A	245	VSS
30	DQ16_A	102	VSS	174	VSS	246	DQ2_B
31	VSS	103	DQ1_B	175	DQ18_A	247	VSS
32	DQ17_A	104	VSS	176	VSS	248	DQ3_B
33	VSS	105	DQS0_B_c	177	DQ19_A	249	VSS
34	DQS2_A_c	106	DQS0_B_t	178	VSS	250	DM0_B_n
35	DQS2_A_t	107	VSS	179	DM2_A_n	251	VSS

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36	VSS	108	DQ4_B	180	VSS	252	DQ6_B
37	DQ20_A	109	VSS	181	DQ22_A	253	VSS
38	VSS	110	DQ5_B	182	VSS	254	DQ7_B
39	DQ21_A	111	VSS	183	DQ23_A	255	VSS
40	VSS	112	DQ8_B	184	VSS	256	DQ10_B
41	DQ24_A	113	VSS	185	DQ26_A	257	VSS
42	VSS	114	DQ9_B	186	VSS	258	DQ11_B
43	DQ25_A	115	VSS	187	DQ27_A	259	VSS
44	VSS	116	DM1_B_n	188	VSS	260	DQS1_B_c
45	DM3_A_n	117	VSS	189	DQS3_A_c	261	DQS1_B_t
46	VSS	118	DQ12_B	190	DQS3_A_t	262	VSS
47	DQ28_A	119	VSS	191	VSS	263	DQ14_B
48	VSS	120	DQ13_B	192	DQ30_A	264	VSS
49	DQ29_A	121	VSS	193	VSS	265	DQ15_B
50	VSS	122	DQ16_B	194	DQ31_A	266	VSS
51	CB0_A	123	VSS	195	VSS	267	DQ18_B
52	VSS	124	DQ17_B	196	CB2_A	268	VSS
53	CB1_A	125	VSS	197	VSS	269	DQ19_B
54	VSS	126	DQS2_B_c	198	CB3_A	270	VSS
55	DQS4_A_c	127	DQS2_B_t	199	VSS	271	DM2_B_n
56	DQS4_A_t	128	VSS	200	ALERT_n	272	VSS
57	VSS	129	DQ20_B	201	VSS	273	DQ22_B
58	CS0_A_n	130	VSS	202	CS1_A_n	274	VSS
59	VSS	131	DQ21_B	203	VSS	275	DQ23_B
60	CA0_A	132	VSS	204	CA1_A	276	VSS
61	CA2_A	133	DQ24_B	205	CA3_A	277	DQ26_B
62	VSS	134	VSS	206	VSS	278	VSS
63	CA4_A	135	DQ25_B	207	CA5_A	279	DQ27_B
64	CA6_A	136	VSS	208	CA7_A	280	VSS
65	VSS	137	DM3_B_n	209	VSS	281	DQS3_B_c
66	CA8_A	138	VSS	210	CA9_A	282	DQS3_B_t
67	CA10_A	139	DQ28_B	211	CA11_A	283	VSS
68	VSS	140	VSS	212	VSS	284	DQ30_B
69	CA12_A	141	DQ29_B	213	RFU	285	VSS
70	RFU	142	VSS	214	RFU	286	DQ31_B
71	VSS	143	RFU	215	VSS	287	VSS
72	CK0_A_t	144	RFU	216	CK1_A_t	288	RFU

Note:

1. The pin assignment table above is a comprehensive list of all possible pin assignments for DDR5 UDIMM modules.

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Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A	Command address input to channel A.	CA0_B - CA12_B	Command address input to channel B.
CS0_A_n - CS1_A_n	DIMM Rank Select Lines input for channel A.	CS0_B_n - CS1_B_n	DIMM Rank Select Lines input for channel B.
DQ0_A - DQ31_A	DIMM memory data bus for channel A.	DQ0_B - DQ31_B	DIMM memory data bus for channel B.
CB0_A - CB3_A	DIMM ECC check bits for channel A. (For ECC UDIMM)	CB0_B - CB3_B	DIMM ECC check bits for channel B. (For ECC UDIMM)
CK0_A_t, CK1_A_t	SDRAM clock for channel A. (positive line of differential pair)	CK0_B_t, CK1_B_t	SDRAM clock for channel B. (positive line of differential pair)
CK0_A_c, CK1_A_c	SDRAM clock for channel A. (negative line of differential pair)	CK0_B_c, CK1_B_c	SDRAM clock for channel B. (negative line of differential pair)
DQS0_A_t - DQS4_A_t	Data Buffer data strobes in channel A. (positive line of differential pair)	DQS0_B_t - DQS4_B_t	Data Buffer data strobes in channel B. (positive line of differential pair)
DQS0_A_c - DQS4_A_c	Data Buffer data strobes in channel A. (negative line of differential pair)	DQS0_B_c - DQS4_B_c	Data Buffer data strobes in channel B. (negative line of differential pair)
DM0_A_n - DM3_A_n	SDRAM input data mask signal for write data of channel A.	DM0_B_nDM3_B_n	SDRAM input data mask signal for write data of channel B.
VIN_BULK	5 V power input supply pin to the PMIC.	VSS	Power supply return (ground)
PWR_GOOD	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regula tors and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low	PWR_EN	Power Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator.
HSCL	Side-band bus serial bus clock for SPD Hub.	RESET_n	Set Register and SDRAMs to a Known State
HSDA	Side-band bus serial data line for SPD Hub.	ALERT_n	Register ALERT_n output
HSA	Side-band bus Host ID and Hub device type ID selection.	RFU	Reserved for future use

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Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA6_A, CA0_B - CA6_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
PAR_A PAR_B		
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input	DIMM ECC check bits.
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
LBDQ	Output	Loopback Data Output: The Output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HIZ based on MR36:OP[2:0].
ALERT_n	Input/ Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of

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		not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
HSCL	Input	Host SidebandBus bus clock, supplied by the master.
HSDA	Input/ Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
HSA	Input	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
PWR_GOOD	Input/ Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_BULK	Supply	5V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to V_{SS}	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to V_{SS}	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to V_{SS}	-0.3 ~ 1.5	V	1,3,5
TSTG	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; When VDD and VDDQ are less than 500mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in DDR5 Device Operation.

tREFI parameters for REFab and REFsb Commands

Command	Refresh Mode	Symbol & Reange		Expression	Value	Unit	Note
REFab	Normal	tREFI1	0°C <= TCASE <= 85°C	rREFI	3.9	us.	
			85°C < TCASE<= 95°C	rREFI/2	1.95	us.	
REFab	Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	rREFI/2	1.95	us.	
			85°C < TCASE<= 95°C	rREFI/4	0.975	us.	
REFsb	Fine Granularity	tREFIsb	0°C <= TCASE <= 85°C	rREFI/(2*n)	1.95/n	us.	1
			85°C < TCASE<= 95°C	rREFI/(4*n)	0.975/n	us.	1

Note:

1. n is the number of banks in a bank group (eg. 8G: n=2; 16G: n=4).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067(-3%)	1.1	1.166(+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067(-3%)	1.1	1.166(+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746(-3%)	1.8	1.908(+6%)	V	10	mOhm	20	mOhm	3

Notes:

1. VDD must be within 66mv of VDDQ.
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

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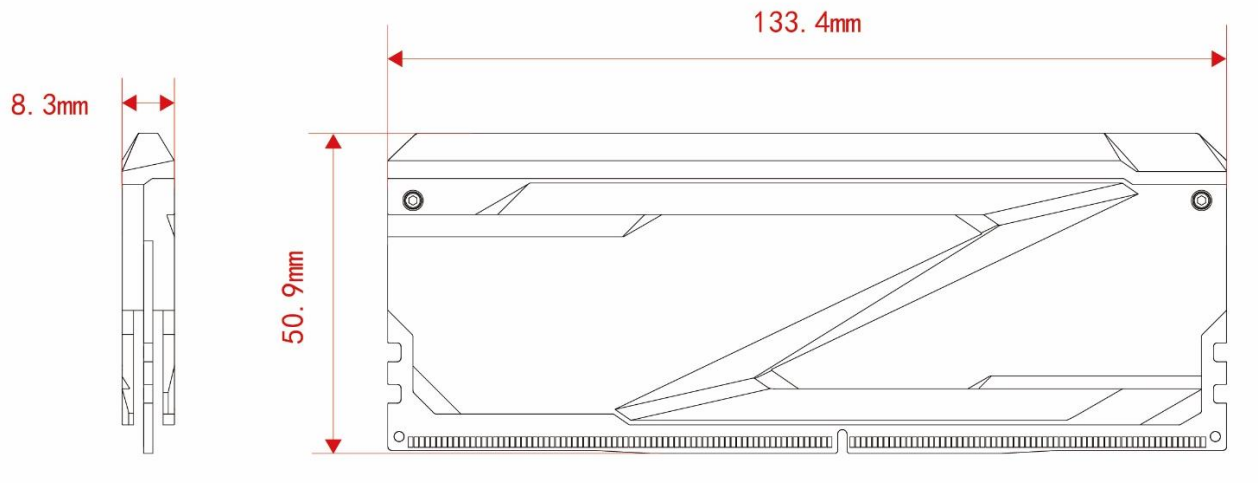
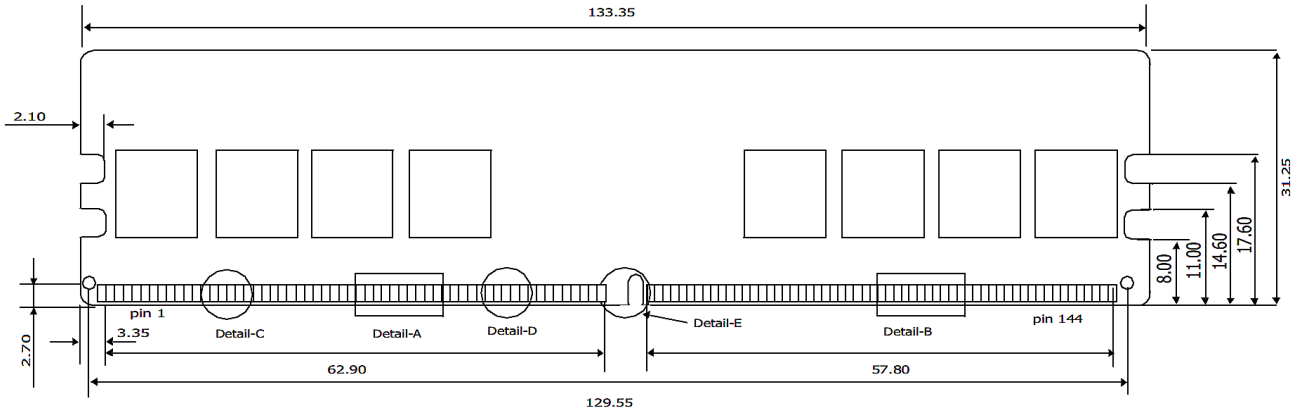
Module With Heat Spreader

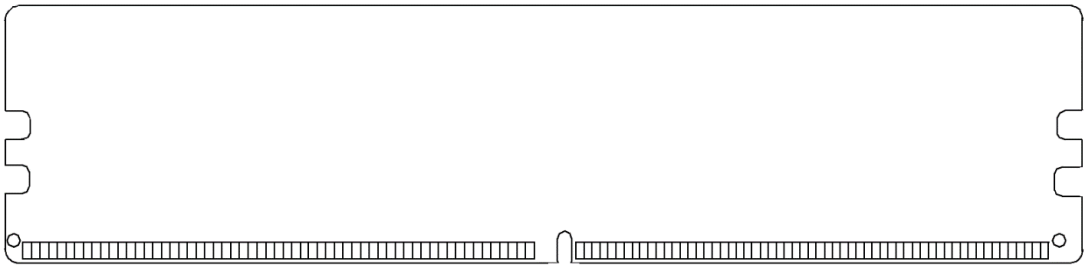


Module Dimensions

Front view



Back view



Notes:

1. All dimensions are in millimeters.
2. Tolerance on all dimensions ±0.15mm unless otherwise specified.
3. The dimensional diagram is for reference only.

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