Basic DDR3 UDIMM
Memory Module Specifications

Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	May.2022	

Ordering Information Table

Model	Type	Capacity	Speed	Latency	Voltage
NTBSD3P16SP-08	DDR3 UDIMM	8GB	1600MHz	11-11-11-28	1.5V
NTBSD3P16SP-04	DDR3 UDIMM	4GB	1600MHz	11-11-11-28	1.5V

Description

Netac Unbuffered DDR3 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR3 SDRAM devices. The SPD is programmed to JEDEC standard latency DDR3-1600 timing of 11-11-11 at 1.5V. Each 240-pin DIMM uses gold contact fingers. The SDRAM Unbuffered DIMM is intended for use as main memory when installed in systems such as PCs.

Features

- Power Supply: VDD=1.5V (1.425V to 1.575V)
- VDDQ = 1.5V (1.425V to 1.575V)
- 800MHz fCK for 1600Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 11, 10, 9, 8, 7, 6
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with t_{CCD} = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal (self) calibration; Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95°C
- Asynchronous Reset
- Adjustable data-output drive strength
- Fly-by topology
- PCB : Height 1.18” (30mm)
- RoHS Compliant and Halogen-Free

Pin Assignments

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	61	A2	121	VSS	181	A1
2	VSS	62	VDD	122	DQ4	182	VDD
3	DQ0	63	NF	123	DQ5	183	VDD
4	DQ1	64	NF	124	VSS	184	CK0
5	VSS	65	VDD	125	DM0	185	CK0#
6	DQS0#	66	VDD	126	NC	186	VDD
7	DQS0	67	VREFCA	127	VSS	187	NC
8	VSS	68	NC	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDD
12	DQ8	72	VDD	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	VSS	193	S0#
14	VSS	74	CAS#	134	DM1	194	VDD
15	DQS1#	75	VDD	135	NC	195	ODT0
16	DQS1	76	NC	136	VSS	196	A13
17	VSS	77	NC	137	DQ14	197	VDD
18	DQ10	78	VDD	138	DQ15	198	NC
19	DQ11	79	NC	139	VSS	199	VSS
20	VSS	80	VSS	140	DQ20	200	DQ36
21	DQ16	81	DQ32	141	DQ21	201	DQ37
22	DQ17	82	DQ33	142	VSS	202	VSS
23	VSS	83	VSS	143	DM2	203	DM4
24	DQS2#	84	DQS4#	144	NC	204	NC
25	DQS2	85	DQS4	145	VSS	205	VSS
26	VSS	86	VSS	146	DQ22	206	DQ38
27	DQ18	87	DQ34	147	DQ23	207	DQ39
28	DQ19	88	DQ35	148	VSS	208	VSS
29	VSS	89	VSS	149	DQ28	209	DQ44
30	DQ24	90	DQ40	150	DQ29	210	DQ45
31	DQ25	91	DQ41	151	VSS	211	VSS
32	VSS	92	VSS	152	DM3	212	DM5
33	DQS3#	93	DQS5#	153	NC	213	NC
34	DQS3	94	DQS5	154	VSS	214	VSS
35	VSS	95	VSS	155	DQ30	215	DQ46
36	DQ26	96	DQ42	156	DQ31	216	DQ47

37	DQ27	97	DQ43	157	VSS	217	VSS
38	VSS	98	VSS	158	NC	218	DQ52
39	NC	99	DQ48	159	NC	219	DQ53
40	NC	100	DQ49	160	VSS	220	VSS
41	VSS	101	VSS	161	NC	221	DM6
42	NC	102	DQS6#	162	NC	222	NC
43	NC	103	DQS6	163	VSS	223	VSS
44	VSS	104	VSS	164	NC	224	DQ54
45	NC	105	DQ50	165	NC	225	DQ55
46	NC	106	DQ51	166	VSS	226	VSS
47	VSS	107	VSS	167	NC	227	DQ60
48	NC	108	DQ56	168	RESET#	228	DQ61
49	NC	109	DQ57	169	NC	229	VSS
50	CKE0	110	VSS	170	VDD	230	DM7
51	VDD	111	DQS7#	171	NF/A151	231	NC
52	BA2	112	DQS7	172	NF/A142	232	VSS
53	NC	113	VSS	173	VDD	233	DQ62
54	VDD	114	DQ58	174	A12	234	DQ63
55	A11	115	DQ59	175	A9	235	VSS
56	A7	116	VSS	176	VDD	236	VDDSPD
57	VDD	117	SA0	177	A8	237	SA1
58	A5	118	SCL	178	A6	238	SDA
59	A4	119	SA2	179	VDD	239	VSS
60	VDD	120	VTT	180	A3	240	VTT

Note: Pin 171 is NF for 1GB and 2GB; A14 for 4GB. Pin 172 is NF for 1GB; A14 for 2GB and 4GB.

Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx,	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are

CKx#		sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-alig
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
VDD	Supply	**Power supply:** 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component VDD and VDDQ are connected to the module VDD.
VDDSPD	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.

VREFCA	Supply	**Reference voltage:** Control, command, and address VDD/2.
VREFDQ	Supply	**Reference voltage:** DQ, DM VDD/2.
VSS	Supply	Ground.
VTT	Supply	**Termination voltage:** Used for control, command, and address VDD/2.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

Notes: The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.283	1.35	1.45	V	
			1.425	1.5	1.575	V	1
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	2
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	–32	0	32	µA	
		S#, CKE, ODT, CK, CK#	-16	0	16		
		DM	–4	0	4		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	-10	0	10	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–16	0	16	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	3
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	3, 4

Notes:

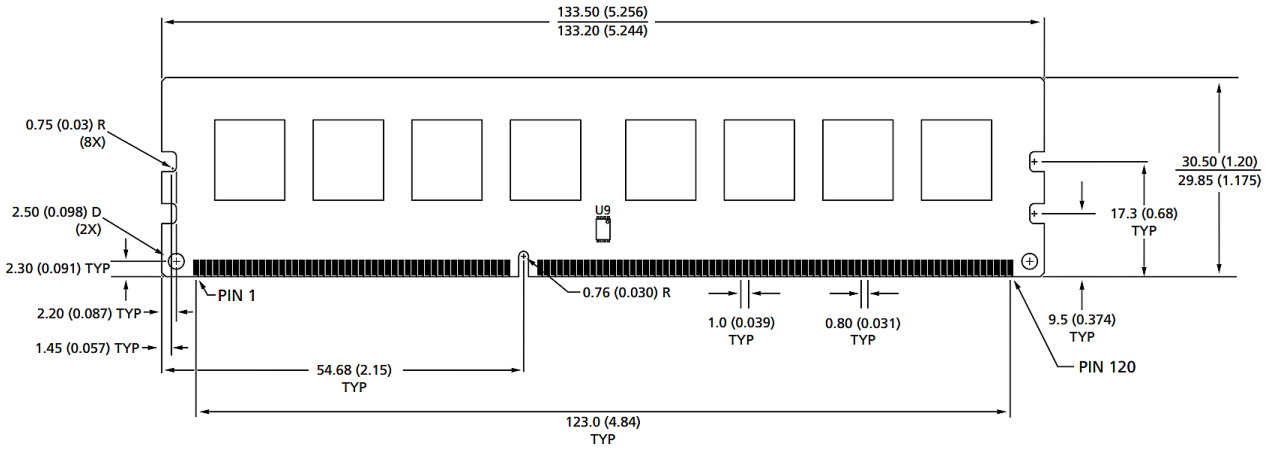
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
2. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
3. T_A and T_C are simultaneous requirements.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

Absolute Maximum Ratings

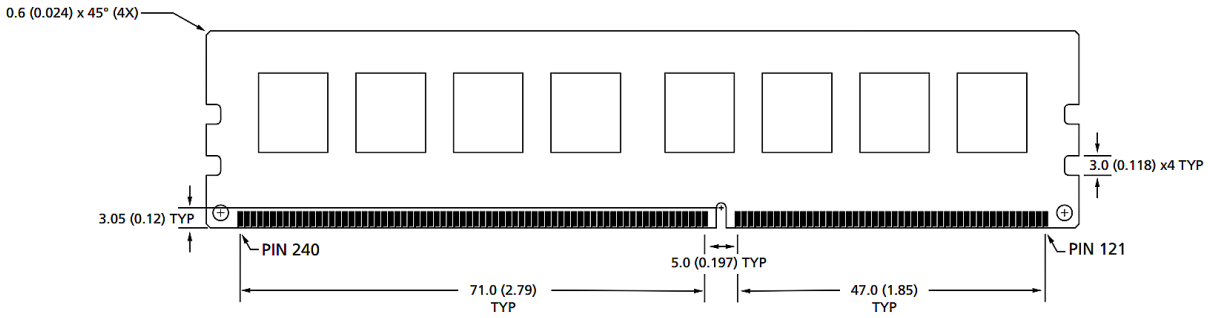
Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.975	V

Module Dimensions

Front view



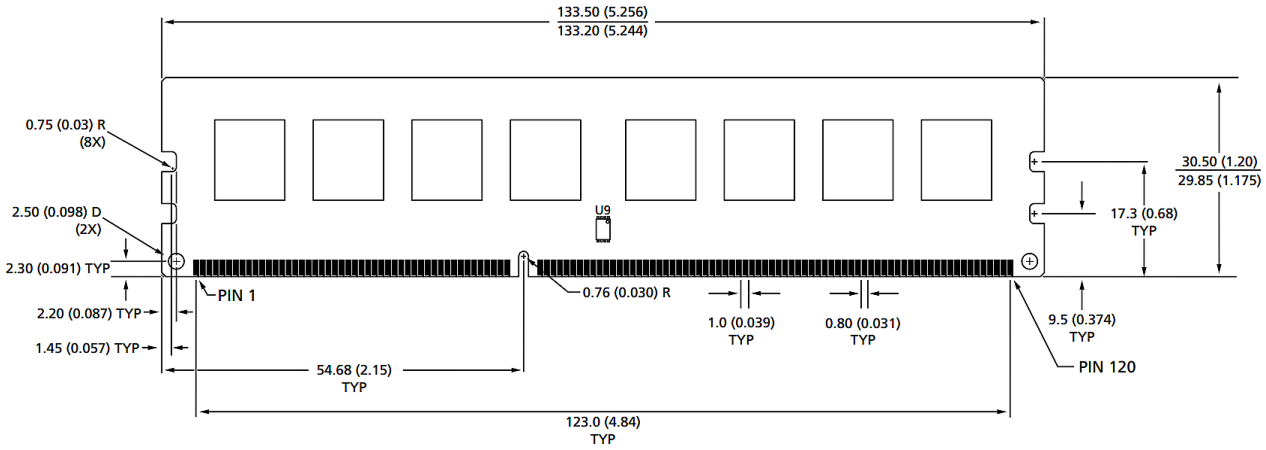
Back view



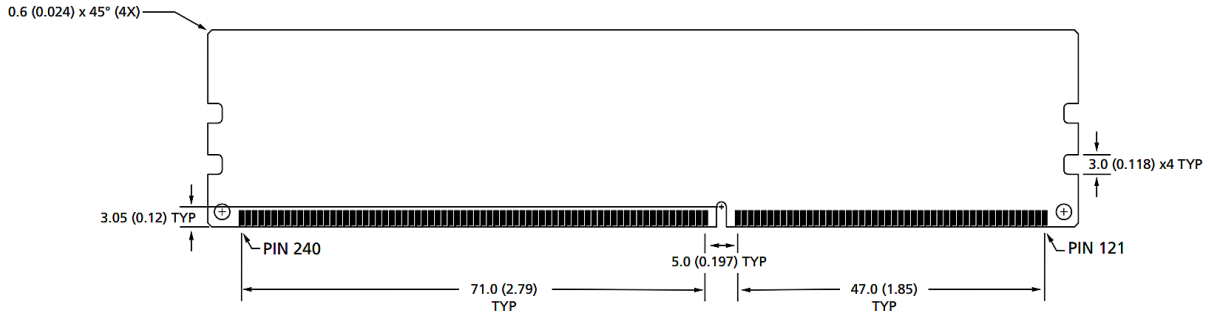
Notes:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15mm unless otherwise specified.
3. The dimensional diagram is for reference only.

Front view



Back view



Notes:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15mm unless otherwise specified.
3. The dimensional diagram is for reference only.